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EXAMINER	
MALEK, LEILA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,031	SUTARDJA ET AL.	
	Examiner	Art Unit	
	Leila Malek	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-94,97-113,115 and 116* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63,67-94,97-106,109-113,115 and 116* is/are rejected.

7)☒ Claim(s) *64-66,107 and 108* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/17/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 03/30/2007 have been fully considered but they are not persuasive.

Applicant's Arguments: Applicant argues that Alelyunas does not disclose updating the LE and/or DFE coefficients with a filtered data term.

Examiner's Response: Examiner asserts that Alelyunas shows the coefficients of the filters have been updated with the filtered error term (see Fig. 5). Alelyunas further shows that the error signal is generated relative to the difference between the determined states of the decision mechanism of the DFE and the filtered communication signals from the LE (See Fig. 5 and column 2, last paragraph). Therefore, inherently since the error signal has been generated based on the filtered data signal, the coefficients of the filters have been updated with the filtered data signal as well.

Drawings

2. The amended drawings have not been received. Therefore the objection to the drawings has been maintained by the Examiner.

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 19 is objected to because of the following informalities: in claim 19, "coefficients are derived from comprises" is vague. Appropriate correction is required.

4. Claims 31 and 72 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 7, 8, 10, 12-15, 30-36, 38, 40-43, 49-52, 58-61, 67, 71, 72, 74-76, 82-86, 91, 93, 94, 97-99, and 109, 111-113, and 115, are rejected under 35 U.S.C. 102(b) as being anticipated by Alelyunas et al. (hereafter, referred as Alelyunas) (US 6,285,709).

As to claim 1, Alelyunas discloses a method for determining an adaptive algorithm (see column 2, last paragraph) for processing data, comprising the steps of: (a) receiving a data sequence 82 in a filter 86 and processing the data sequence in

accordance with coefficients in the filter (see Fig. 5, the abstract) to produce a processed data sequence (i.e. output of the equalizer 86); (b) filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the coefficients (see linear equalizer); (c) generating a filtered error term (see error signal 94) for the coefficients from at least the processed data sequence using a second set of filter characteristics (i.e. the DFE equalizer 90), wherein the second set of filter characteristics being functionally identical (they are both equalizers, so they have the same (identical) functionally) to the first set of filter characteristics; and (d) updating the coefficients in the filter with each of the filtered data term and the filtered error term (see Fig. 5 and column 2, last paragraph (Alelyunas shows the coefficients of the filters have been updated with the filtered error term (see Fig. 5). Alelyunas further shows that the error signal is generated relative to the difference between the determined states of the decision mechanism of the DFE and the filtered communication signals from the LE (See Fig. 5 and column 2, last paragraph). Therefore, inherently since the error signal has been generated based on the filtered data signal, the coefficients of the filters have been updated with the filtered data signal as well.)).

As to claims 30 and 31, Alelyunas discloses a method for determining an adaptive algorithm (see column 2, last paragraph) for processing data, comprising the steps of: (a) processing a data sequence in accordance with the coefficients in the filter (see Fig. 5, the abstract) to produce a processed data sequence (i.e. output of the equalizer 86); (b) filtering the data sequence to generate a filtered data term for coefficients using the first set of filter characteristics (see linear equalizer); (c) filtering

an error term for the coefficients generated from at least the processed data sequence (see Fig. 5), using second set of filter characteristics functionally identical to the first set of filter characteristics (they are both equalizers, so they have the same (identical) functionally); and (d) updating the coefficients in the filter with each of the filtered data term and the filtered error term (see Fig. 5 and column 2, last paragraph (Alelyunas shows the coefficients of the filters have been updated with the filtered error term (see Fig. 5). Alelyunas further shows that the error signal is generated relative to the difference between the determined states of the decision mechanism of the DFE and the filtered communication signals from the LE (See Fig. 5 and column 2, last paragraph). Therefore, inherently since the error signal has been generated based on the filtered data signal, the coefficients of the filters have been updated with the filtered data signal as well.)).

As to claims 49, 72, and 74, Alelyunas discloses an apparatus, comprising: (a) an equalizer 86 configured to equalize a data sequence in accordance with filter coefficients and provide an equalized data output (see the abstract); (b) a first filter (i.e. the combined FIR filter (filters 86 and 102), configured to receive the data sequence and generate a filtered data term for updating the filter coefficients; and (c) an error term circuit (see filters 90 and 108), configured to receive the equalized data output and provide a filtered error term 94 for updating the filter coefficients, the error term circuit comprising a second filter 90 having filter characteristics functionally identical to the first filter (they are both equalizers, so they have the same (identical) functionally).

As to claim 2, Alelyunas discloses that step (c) comprises convolving the processed data sequence with the second set of filter characteristics to generate a filtered processed data sequence (see Fig. 2 and Fig. 4, lines 27-21).

As to claims 3, 7, and 35, Alelyunas further discloses that step (c) further comprises determining a difference between the filtered processed data sequence (see Fig. 2) and an ideal filtered processed data (i.e. the output of the Decision Mechanism device) sequence to produce the filtered error term.

As to claims 8 and 36, Alelyunas further discloses that step (c) further comprises convolving the error term with the second set of filter characteristics (DFE) to generate the filtered error term (see Fig. 5).

As to claims 10, 38, 67, and 91, Alelyunas further discloses that each of the first and second sets of filter characteristics comprises an error filter (see Filters 102 and 108).

As to claims 12 and 40, Alelyunas further discloses that the data sequence comprises a digital data signal (see column 4, line 14).

As to claims 13 and 41, Alelyunas further discloses step a) comprises equalizing the data sequence, wherein the processed data sequence comprises an equalized data signal (see Fig. 5), the filtered processed data sequence comprises a filtered equalized data signal, and an ideal filtered processed data sequence comprises an ideal filtered equalized data signal.

As to claims 14, 42, and 93, Alelyunas further discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19).

As to claims 15, 43, and 94, Alelyunas discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19). Inherently, this error must be at least a single bit error.

As to claim 32, Alelyunas further discloses that the filtering step (c) comprises convolving the processed data sequence with a first filter comprising the set of filter characteristics to generate a filtered processed data sequence (see Fig. 5).

As to claim 34, Alelyunas discloses that step (c) comprises (i) detecting a sequence of the processed data sequence (receiving the processed data sequence by DFE has been interpreted as detecting a sequence of the processed data sequence) (ii) convolving the processed data sequence with the second set of filter characteristics to generate a filtered processed data sequence (see Fig. 2 and Fig. 4, lines 27-21).

As to claims 50, 75, and 98, Alelyunas further discloses that the equalizer comprises an adaptive finite impulse response filter (see column 3, lines 40-44).

As to claim 51 and 99, Alelyunas further discloses that the filter coefficients are derived from a least-mean-squares (LMS) gradient algorithm (see column 4, line 17).

As to claims 52 and 76, Alelyunas further discloses that the error term circuit further comprises a signal processor configured to receive the equalized data output (see Fig. 5 and line 14-16).

As to claims 33 and 58, Alelyunas further discloses that step (c) further comprises determining a difference between the filtered processed data sequence (see Fig. 2) and an ideal filtered processed data (i.e. the output of the Decision Mechanism device) sequence to produce the filtered error term.

As to claim 59, Alelyunas further discloses that the subtractor is configured to subtract one of the equalized data output and the ideal equalized data output from the other of the equalized data output and the ideal equalized data output (see Fig. 5).

As to claim 60, Alelyunas further discloses that the second filter receives the error term and provides a filtered equalized data output (see Fig. 5).

As to claims 61, Alelyunas discloses that the second filter receives the equalized data output and provides a filtered equalized data output (see Fig. 5).

As to claim 71, Alelyunas discloses that the apparatus is comprising a receiver to receive data from a magnetic storage and provide the data sequence (see column 1, line 26).

As to claim 82, Alelyunas further discloses a means for providing an error term, configured to receive the equalized data signal and an ideal equalized data signal (see Fig. 5).

As to claim 83, Alelyunas further discloses that the subtractor is configured to subtract one of the equalized data output and the ideal equalized data output from the other of the equalized data output and the ideal equalized data output (see Fig. 5).

As to claim 84, Alelyunas further discloses that the second means for filtering receives the error term (see Fig. 5, DFE) and provides the filtered error term.

As to claim 85, Alelyunas further discloses that the second means for filtering receives the equalized data signal and provides a filtered equalized data signal (see Fig. 5).

As to claim 86, Alelyunas discloses that means for providing the filtered error term further comprises a means for processing (i.e. equalizing by the second equalizer) the equalized data signal (see Fig. 5).

As to claims 97 and 115, Alelyunas discloses a system for reading magnetically recorded data, comprising: the architecture of claim 49 (see the rejection for claim 49); and at least one receiver communicatively coupled to the architecture for receiving the first data sequence (see column 1, lines 23-27).

As to claim 109, Alelyunas further discloses that each of the first and second sets of filter characteristics comprises an error filter (see Filters 102 and 108).

As to claim 111, Alelyunas further discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19).

As to claim 112, Alelyunas discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19). Inherently, this error must be at least a single bit error.

As to claims 113, Alelyunas discloses using second set of filter characteristics functionally identical to the first set of filter characteristics (they are both equalizers, so they have the same (identical) functionally).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16-28, and 29, 44-48, 69, 70, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alelyunas.

As to claims 17 and 44, Alelyunas discloses a method for determining an adaptive algorithm (see column 2, last paragraph) for processing data, comprising the steps of: (a) processing a data sequence in accordance with the coefficients in the filter (see Fig. 5, the abstract) to produce a processed data sequence (i.e. output of the equalizer 86); (b) filtering the data sequence to generate a filtered data term for coefficients using the first set of filter characteristics (see linear equalizer); (c) filtering an error term for the coefficients generated from at least the processed data sequence (see Fig. 5), using second set of filter characteristics functionally identical to the first set of filter characteristics (they are both equalizers, so they have the same (identical) functionally); and (d) (d) updating the coefficients in the filter with each of the filtered data term and the filtered error term (see Fig. 5 and column 2, last paragraph (Alelyunas shows the coefficients of the filters have been updated with the filtered error term (see Fig. 5). Alelyunas further shows that the error signal is generated relative to the difference between the determined states of the decision mechanism of the DFE and the filtered communication signals from the LE (See Fig. 5 and column 2, last paragraph). Therefore, inherently since the error signal has been generated based on

the filtered data signal, the coefficients of the filters have been updated with the filtered data signal as well.)). Alelyunas does not expressly disclose a computer-readable medium or waveform containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform the method of claim 1. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use a computer-readable medium to store a set of instructions and transfer such instructions to the receiver to carry out the data processing on the received signal.

As to claims 18 and 45, Alelyunas further discloses that the coefficients are for an adaptive finite impulse response (FIR) algorithm (see column 3, lines 40-44).

As to claims 19 and 46, Alelyunas further discloses that the coefficients are derived from a least-mean-squares (LMS) gradient algorithm (see column 4, line 17).

As to claim 20, Alelyunas further discloses that processing step a) comprises equalizing the data sequence (see Fig. 5).

As to claim 21, Alelyunas discloses that step (c) comprises (i) detecting a sequence of the processed data sequence (receiving the processed data sequence by DFE has been interpreted as detecting a sequence of the processed data sequence) (ii) convolving the processed data sequence with the second set of filter characteristics to generate a filtered processed data sequence (see Fig. 2 and Fig. 4, lines 27-21).

As to claims 22 and 23, Alelyunas further discloses that step (c) further comprises determining a difference between (i.e. subtracting) the filtered processed

data sequence (see Fig. 2) and an ideal filtered processed data (i.e. the output of the Decision Mechanism device) sequence to produce the filtered error term.

As to claim 24, Alelyunas further discloses that step (c) further comprises convolving the error term with the second set of filter characteristics (DFE) to generate the filtered error term (see Fig. 5).

As to claim 25, Alelyunas further discloses that each of the first and second sets of filter characteristics comprises an error filter (see Filters 102 and 108).

As to claims 26 and 69, Alelyunas further discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19).

As to claims 70, Alelyunas discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19). Inherently, this error must be at least a single bit error.

As to claim 16, Alelyunas discloses that the first and second sets of filter characteristics are configured to minimize a dominant error type (see column 4, lines 17-19). Although Alelyunas does not expressly disclose that the error is a dibit error, however it would have been clearly recognizable to one of ordinary skill in the art that the error could be a signal bit error or a multi-bit error.

As to claim 27, Alelyunas further discloses that the first set of filter characteristics is identical to the second set of filter characteristics (see column 4, lines 27-30).

As to claims 28 and 47, Alelyunas further discloses that the data sequence comprises a digital data signal (see column 4, line 14). Therefore, inherently the set of instructions comprises binary code.

As to claims 29 and 48, Alelyunas further discloses that the data sequence comprises a digital data signal (see column 4, line 14).

As to claim 116, Alelyunas discloses all the subject matters claimed in claim 116, except that the computer has a hard disk drive. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use a hard disk drive in a computer system to store and retrieve the information.

7. Claims 4-6, 9, 37, 53-57, 62, 63, 73, 77-81, 87- 89,100-102, and 104-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alelyunas, in view of background of invention.

As to claims 4 and 9, Alelyunas discloses all the subject matters claimed in claims 3, 7 except that the method further comprising: convolving the detected processed data sequence with a third set of filter characteristics to generate the ideal filtered processed data sequence. Applicant in the background of invention shows that the output of the FIR filter 12 has been detected by sequence detector 14. Applicant in the background of invention further discloses convolving the detected processed data sequence with a third set of filter characteristics to generate the ideal filtered processed data sequence (see Target filter 16). It would have been obvious to one of ordinary skill in the art at the time of invention to use a sequence detector and a target filter to generate an ideal, noiseless data signal from the equalizers (see paragraph 0003).

As to claims 5, Alelyunas further discloses that the first set of filter characteristics is identical to the second set of filter characteristics (see column 4, lines 27-30).

As to claims 53, 77, and 100, Alelyunas discloses all the subject matters claimed in claims 53, 77, and 100, except that the signal processor comprises a sequence detector configured to provide a sequence detected equalized data output. Applicant in the background of invention shows that the output of the FIR filter 12 has been detected by sequence detector 14. Applicant in the background of invention further discloses convolving the detected processed data sequence wit ha third set of filter characteristics to generate the ideal filtered processed data sequence (see Target filter 16). It would have been obvious to one of ordinary skill in the art at the time of invention to use a sequence detector to generate an ideal, noiseless data signal from the equalizers (see paragraph 0003).

As to claims 37 and 101, Alelyunas discloses all the subject matters claimed in claims 37 and 101, except that the method further comprising: convolving the detected processed data sequence with a third set of filter characteristics to generate the ideal filtered processed data sequence. Applicant in the background of invention shows that the output of the FIR filter 12 has been detected by sequence detector 14. Applicant in the background of invention further discloses convolving the detected processed data sequence with a third set of filter characteristics to generate the ideal filtered processed data sequence (see Target filter 16). It would have been obvious to one of ordinary skill in the art at the time of invention to use a sequence detector and a target filter to generate an ideal, noiseless data signal from the equalizers (see paragraph 0003).

As to claim 104, Alelyunas further discloses that step (c) further comprises determining a difference between the filtered processed data sequence (see Fig. 2) and an ideal filtered processed data (i.e. the output of the Decision Mechanism device) sequence to produce the filtered error term.

As to claim 105, Alelyunas further discloses that the second filter receives the error term and provides a filtered equalized data output (see Fig. 5).

As to claims 106, Alelyunas discloses that the second filter receives the equalized data output and provides a filtered equalized data output (see Fig. 5).

As to claim 89, Alelyunas further shows (see Fig. 5) that the apparatus further comprises a means for generating the filtered error term, configured to receive the filtered equalized data signal and the ideal filtered equalized data signal (i.e. output of the decision mechanism).

As to claims 6, 56, 73, 80, and 102, since equalizers and filters have the same functionality, inherently, the third set of filter characteristics comprising a subset of filter characteristics functionally identical to the first and second sets of filter characteristics.

As to claim 54, 55, 57, 62, 63, 78, 79, 81, 87, 88, and 103, Alelyunas discloses all the subject matters claimed in the above claims, except that the signal processor comprises a sequence detector configured to provide a sequence detected equalized data output. Applicant in the background of invention shows that the output of the FIR filter 12 has been detected by sequence detector 14. Applicant in the background of invention further discloses convolving the detected processed data sequence with a third set of filter characteristics (i.e. a target filter) to generate the ideal filtered

processed data sequence (see Target filter 16). It would have been obvious to one of ordinary skill in the art at the time of invention to use a sequence detector and a target filter to generate an ideal, noiseless data signal from the equalizers (see paragraph 0003).

As to claim 90, Alelyunas further discloses that the subtractor is configured to subtract one of the equalized data output and the ideal equalized data output from the other of the equalized data output and the ideal equalized data output (see Fig. 5).

8. Claims 11 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alelyunas, in view of Lu (US 6,768,796).

As to claims 11 and 39, Alelyunas discloses all the subject matters claimed in claim 10 and 38, except that filtering further comprises transposing a channel response to generate at least a subset of the first set of filter characteristics. Lu, discloses a method and system for echo (noise, error) cancellation in a communication network (see the abstract). Lu further discloses that an adaptive filter 408 generates and updates filter tap coefficients vector 408 to model the characteristics impulse response of the echo channel 402, so that the far end signal can be adaptively filtered to create a local replica of the far end echo, or an echo estimate signal (See column 8, lines 29-38). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Alelyunas as suggested by Lu to estimate the echo signal and therefore cancel the noise (echo) more accurately.

9. Claims 68, 92, and 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alelyunas, in view of Xia et al. (hereafter, referred as Xia) (US 2002/0097795).

As to claims 68, 92, and 110, Alelyunas discloses all the subject matters claimed, except that the first and second filters comprise a matched filter. Xia, in the same field of endeavor, discloses an equalizer 120 which comprises a matched filter 321 (see Fig. 3) to permit synchronization even with multiple, arbitrarily strong ghosts caused by strong multi-pathing, multiple transmitters, or both. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Alelyunas as suggested by Xia for the reasons stated above.

Allowable Subject Matter

10. Claims 64-66, 107, and 108 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leila Malek whose telephone number is 571-272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

L.M.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER